## **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((overlap\$3 or congest\$3 or shar\$3 or infeasible) with (connect\$3 or wir\$3 or interconnect\$3) same (remov\$3 or eliminat\$3 or tak\$3 or exclud\$3 or delet\$3) and (delay or timing) and (predict\$3 or estimat\$3 or evaluat\$3 or calculat\$3 or comput\$3 gues\$4) and rout\$3).clm. and "716"/\$.ccls.	US-PGPUB	OR	ON	2006/09/29 16:09



Home | Login | Logout | Access Information | Aler Sitemap | H

Welcome United States Patent and Trademark Office

□ Search Results

**BROWSE SEARCH** 

**IEEE XPLORE** GUIDE

SUPPOR'

Results for "(((timing or delay) and (driven or based) and (global routing)and congest\* and (predict\* or estimat\*..."
Your search matched 7 of 488547 documents.

☑e-mail 🚇 printer i

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

## » Search Options

View Session History New Search

## **Modify Search**

Display

Format:

(((timing or delay) and (driven or based) and (global routing)and congest\* and (pred Sea

Check to search only within this results set

» Key IEEE

JNL

IEEE Journal or Magazine

IEE Journal or IEE JNL Magazine

IEEE IEEE CNF

Conference

Proceeding

IEE CNF IEE

Conference

Proceeding

IEEE STD IEEE Standard d view selected items

Select All Deselect

© Citation © Citation & Abstract

1. Maple-opt: a performance-oriented simultaneous technology mapping, placement, and global routing algorithm for FPGAs Togawa, N.; Yanagisawa, M.; Ohtsuki, T.; Computer-Aided Design of Integrated Circuits and Systems, IEEE

Transactions on Volume 17, Issue 9, Sept. 1998 Page(s):803 - 818 Digital Object Identifier 10.1109/43.720317

AbstractPlus | References | Full Text: PDF(496 KB)

Rights and Permissions

2. An effective congestion-driven placement framework
Brenner, U.; Rohe, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE
Transactions on
Volume 22, Issue 4, April 2003 Page(s):387 - 394
Digital Object Identifier 10.1109/TCAD.2003.809662 

AbstractPlus | References | Full Text: PDF(831 KB) | IEEE JNL Rights and Permissions

3. Multilevel global placement with congestion control Chin-Chih Chang; Cong, J.; Zhigang Pan; Xin Yuan; Computer-Aided Design of Integrated Circuits and Systems, IEEE

Transactions on Volume 22, Issue 4, April 2003 Page(s):395 - 409 Digital Object Identifier 10.1109/TCAD.2003.809661

AbstractPlus | References | Full Text: PDF(839 KB) Rights and Permissions **IEEE JNL** 

<sup>4.</sup> Semi-individual wire-length prediction with application to logi synthesis

Qinghua Liu; Marek-Sadowska, M.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on

http://ieeexplore.ieee.org/search/searchresult.jsp?query1=&scope1=metadata&op1=and&quer... 9/29/2006

Volume 25, Issue 4, April 2006 Page(s):611 - 624 Digital Object Identifier 10.1109/TCAD.2005.859487 <u>AbstractPlus</u> | Full Text: <u>PDF</u>(584 KB) **IEEE JNL** Rights and Permissions

5. Single-layer global routing
Sarrafzadeh, M.; Kuo-Feng Liao; Wong, C.K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE
Transactions on
Volume 13, Issue 1, Jan. 1994 Page(s):38 - 47
Digital Object Identifier 10.1109/43.273751
AbstractPlus | Full Text: PDF(872 KB) IEEE JNL
Rights and Permissions

6. Multilayer chip-level global routing using an efficient graph-basteiner tree heuristic
Liu, L.-C.E.; Sechen, C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE
Transactions on
Volume 18, Issue 10, Oct 1999 Page(s):1442 - 1451
Digital Object Identifier 10.1109/43.790621
AbstractPlus | Full Text: PDF(323 KB) IEEE JNL
Rights and Permissions

7. Algorithms for an FPGA switch module routing problem with application to global routing
Thakur, S.; Yao-Wen Chang; Wong, D.F.; Muthukrishnan, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 16, Issue 1, Jan. 1997 Page(s):32 - 46
Digital Object Identifier 10.1109/43.559330

AbstractPlus | References | Full Text: PDF(476 KB) IEEE JNL Rights and Permissions

Help Contact Us Priva Security IEEE © Copyright 2006 IEEE Rights Resa

**週 lusbec.**